

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

Docket No.: P12006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: John Alan Miller et al.

Group Art Unit: 2111

Application No.: 10/032,565

Examiner: KENNETH S. KIM

Filed: January 2, 2002

For: TRACE CACHE BYPASSING

RECEIVED
CENTRAL FAX CENTER

AUG - 2 2004

OFFICIAL

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Non-fee Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Restriction Requirement mailed on July 2, 2004, Applicants submit the following:

IN THE CLAIMS:

The status of the claims is as follows:

1. (Original) A method of managing processor instructions, the method comprising:
decoding a first instruction into a plurality of operations with a decoder;
passing a first copy of the operations from the decoder to a build engine associated with a trace cache; and
passing a second copy of the operations from the decoder directly to a back end allocation module, the operations bypassing the build engine and the allocation module being in a decoder reading state.
2. (Currently Amended) The method of claim 1 further including:
determining at the decoder whether a resume condition is present based on a second instruction; and
switching the allocation module from the decoder reading state to a trace cache reading state if [when] the resume condition is present.
3. (Original) The method of claim 2 further including searching the trace cache for an instruction pointer that corresponds to the second instruction.
4. (Original) The method of claim 3 further including repeating the searching for every subsequent instruction decoded by the decoder.

Docket No.: P12006

5. (Original) The method of claim 3 further including repeating the searching for a subset of every subsequent instruction decoded by the decoder.

6. (Original) The method of claim 5 further including selecting the subset based on a lookup to an abbreviated tag array.

7. (Original) The method of claim 5 further including selecting the subset based on an instruction heuristic.

8. (Original) The method of claim 7 further including determining whether an immediately preceding instruction was a branch instruction.

9. (Original) The method of claim 1 further including passing the second copy to a buffer of the allocation module.

10. (Withdrawn) A method of managing processor instructions, the method comprising:

determining at a decoder whether a resume condition is present based on an instruction;

and

switching a backend allocation module of a processor from a decoder reading state to a trace cache reading state when the resume condition is present.

11. (Withdrawn) The method of claim 10 further including searching the trace cache for an instruction pointer that corresponds to the instruction.

12. (Withdrawn) The method of claim 11 further including repeating the searching for every subsequent instruction decoded by the decoder.

13. (Withdrawn) The method of claim 11 further including repeating the searching for a subset of every subsequent instruction decoded by the decoder.

14. (Withdrawn) The method of claim 13 further including selecting the subset based on a lookup to an abbreviated tag array.

15. (Withdrawn) The method of claim 13 further including selecting the subset based on an instruction heuristic.

16. (Currently Amended) A method of managing instructions in a computer processing architecture having a trace cache, the method comprising:

detecting a trace cache miss;

receiving a first instruction;

decoding the first instruction into a plurality of operations with a decoder;

passing a first copy of the operations from the decoder to a build engine associated with the trace cache;

passing a second copy of the operations from the decoder directly to a back end

Docket No.: P12006

allocation module, the operations bypassing the build engine and the allocation module being in a decoder reading state;

receiving a second instruction;

determining at the decoder whether a resume condition is present based on the second instruction; and

switching the allocation module from the decoder reading state to a trace cache reading state if [when] the resume condition is present.

17. (Original) The method of claim 16 further including searching the trace cache for an instruction pointer that corresponds to the second instruction.

18. (Original) The method of claim 17 further including repeating the searching for every subsequent instruction decoded by the decoder.

19. (Original) The method of claim 17 further including repeating the searching for a subset of every subsequent instruction decoded by the decoder.

20. (Original) A processor instruction management system comprising:

a decoder to decode a first instruction into a plurality of operations; and

a controller to pass a first copy of the operations from the decoder to a build engine associated with a trace cache, the controller to pass a second copy of the operations from the decoder directly to an allocation module, the operations bypassing the build engine and the allocation module being in a decoder reading state.

21. (Currently Amended) The instruction management system of claim 20 wherein the controller includes control logic to determine whether a resume condition is present based on a second instruction, the control logic to switch the allocation module from the decoder reading state to a trace cache reading state if [when] the resume condition is present.

22. (Original) The instruction management system of claim 21 wherein the control logic is to search the trace cache for an instruction pointer that corresponds to the second instruction.

23. (Original) The instruction management system of claim 22 wherein the control logic is to repeat the searching for every instruction decoded by the decoder.

24. (Original) The instruction management system of claim 22 wherein the control logic is to repeat the searching for a subset of every instruction decoded by the decoder.

25. (Original) The instruction management system of claim 24 wherein the controller further includes an abbreviate tag array, the control logic selecting the subset based on a lookup to the abbreviated tag array.

26. (Original) The instruction management system of claim 24 wherein the controller further includes an instruction heuristic, the control logic selecting the subset based on the instruction heuristic.

Docket No.: P12006

27. (Original) The instruction management system of claim 26 wherein the instruction heuristic determines whether an immediately preceding instruction was a branch instruction.

28. (Original) The instruction management system of claim 20 wherein the decoder and the controller are part of an application specific integrated circuit (ASIC).

Docket No.: P12006

REMARKS

Claims 1-9 and 16-28 are pending in the present application. By this Response, claims 1-9 and 20-28 (Group I) are elected and claims 10-15 (Group II) are withdrawn, without traverse. Claims 2, 16 and 21 have been amended to clarify that the claimed switching and resume condition need not occur simultaneously. The amendments present no new matter. Allowance of the claims is respectfully requested.

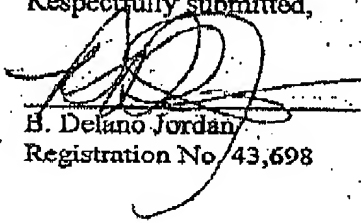
Docket No.: P12006

CONCLUSION

Applicants assert that all claims are in condition for allowance. Applicants respectfully request the Examiner to pass this case to issue at the Examiner's earliest possible convenience.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at 703.633.0962.

Respectfully submitted,

Date: August 2, 2004
B. Delano Jordan
Registration No. 43,698

Intel Americas, Inc.
4030 Lafayette Center Drive
Building LF3
Chantilly, VA 20151

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

By: 

Serita Evans

Date: August 2, 2004